

FORM PTO-1390
(REV. 5-93)U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICEATTORNEY'S DOCKET NUMBER
52433/544TRANSMITTAL LETTER TO THE UNITED STATES
DESIGNATED/ELECTED OFFICE (DO/EO/US)
CONCERNING A FILING UNDER 35 U.S.C. 371

U.S. APPLICATION NO. (If known, see 37 CFR 1.5)

09/254118

INTERNATIONAL APPLICATION NO.
JP97/02988INTERNATIONAL FILING DATE
(27.08.97)
27 August 1997PRIORITY DATES CLAIMED
(27.08.96)
27 August 1996TITLE OF INVENTION
METHOD OF PARTIALLY PLATING SUBSTRATE FOR ELECTRONIC DEVICESAPPLICANT(S) FOR DO/EO/US
TATSUMI, Kohei; SHIMOKAWA, Kenji and HASHINO, Eiji

Applicants herewith submit to the United States Designated/Elected Office (DO/EO/US) the following items and other information

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).
4. ☒ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.
5. ☒ A copy of the International Application as filed (35 U.S.C. 371(c)(2))
 - a. ☐ is transmitted herewith (required only if not transmitted by the International Bureau).
 - b. ☒ has been transmitted by the International Bureau.
 - c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US)
6. ☒ A translation of the International Application into English (35 U.S.C. 371(c)(2)).
7. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))
 - a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
 - b. ☐ have been transmitted by the International Bureau.
 - c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
 - d. ☒ have not been made and will not be made.
8. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. ☐ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4))
10. ☐ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11. to 16. below concern other document(s) or information included:

11. ☒ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included
13. ☒ A **FIRST** preliminary amendment.
☐ A **SECOND** or **SUBSEQUENT** preliminary amendment.
14. ☐ A substitute specification.
15. ☐ A change of power of attorney and/or address letter.
16. ☒ Other items or information: International Search Report and PCT/RO/101.

EXPRESS NO. : EL303285075US
65332

U.S. APPLICATION NO if known, see
37 C.F.R. 1.5

INTERNATIONAL APPLICATION NO

PCT/JP97/02988

ATTORNEY'S DOCKET NUMBER

52433/544

17. ☒ The following fees are submitted:

Basic National Fee (37 CFR 1.492(a)(1)-(5)):

Search Report has been prepared by the EPO or JPO \$840.00

International preliminary examination fee paid to USPTO (37 CFR 1.482) . \$670.00

No international preliminary examination fee paid to USPTO (37 CFR 1.482) but
international search fee paid to USPTO (37 CFR 1.445(a)(2)) \$760.00

Neither international preliminary examination fee (37 CFR 1.482) nor international
search fee (37 CFR 1.445(a)(2)) paid to USPTO \$970.00

International preliminary examination fee paid to USPTO (37 CFR 1.482) and all
claims satisfied provisions of PCT Article 33(2)-(4) \$96.00

CALCULATIONS

PTO USE ONLY

ENTER APPROPRIATE BASIC FEE AMOUNT =

\$ 840.00

Surcharge of \$130.00 for furnishing the oath or declaration later than ☐ 20 ☐ 30
months from the earliest claimed priority date (37 CFR 1.492(e)).

\$

Claims

Number Filed

Number Extra

Rate

Total Claims

9 - 20 =

0

X \$18.00

\$

Independent Claims

1 - 3 =

0

X \$78.00

\$

Multiple dependent claim(s) (if applicable)

+ \$260.00

\$

TOTAL OF ABOVE CALCULATIONS =

\$840.00

Reduction by 1/2 for filing by small entity, if applicable. Verified Small Entity statement
must also be filed. (Note 37 CFR 1.9, 1.27, 1.28).

\$

SUBTOTAL =

\$

Processing fee of \$130.00 for furnishing the English translation later the ☐ 20 ☐ 30
months from the earliest claimed priority date (37 CFR 1.492(f)).

\$

TOTAL NATIONAL FEE =

\$840.00

Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be
accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). \$40.00 per property +

\$

TOTAL FEES ENCLOSED =

\$840.00

Amount to be:
refunded

\$

charged

\$

a. ☐ A check in the amount of \$_____ to cover the above fees is enclosed.

b. ☒ Please charge my Deposit Account No. 11-0600 in the amount of **\$840.00** to cover the above fees. A duplicate copy of this
sheet is enclosed.

c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to
Deposit Account No. 11-0600. A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b))
must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

Kenyon & Kenyon
One Broadway
New York, New York 10004

SIGNATURE

Edward W. Greason, Reg. No. 18,918
NAME

DATE

Feb 25, 1999

09/254118

800 Rec'd PCT/PTO 25 FEB 1999

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

PRELIMINARY AMENDMENT

Docket Number
52433/544International Application
Number

International Filing Date

U.S. Filing Date

Examiner

Art Unit

PCT/JP97/02988

August 27, 1997

Herewith

Invention Title

Inventor(s)

METHOD OF PARTIALLY PLATING SUBSTRATE FOR
ELECTRONIC DEVICES

TATSUMI, Kohei et al.

Assistant Commissioner for Patents
Washington D.C. 20231
Box PCT

SIR:

Please amend the above-referenced patent application as follows:

In the Claims:

In claim 5, line 2, delete "or 2";

In claim 6, line 2, delete "or 2";

In claim 7, line 2, delete "or 2";

In claim 8, line 2, delete "or 2";

In claim 9, line 2, delete "or 2";

Remarks

The specification has been amended in order to eliminate multiple dependent claims.

An early indication of allowable subject matter is respectfully requested.

The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 11-0600. Duplicate copies of this sheet are enclosed herewith.

Dated: Feb 25/1 1999



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Express Mail No. EL303285075US

DESCRIPTION

METHOD OF PARTIALLY PLATING SUBSTRATE FOR
ELECTRONIC DEVICES

5

Technical Field

The present invention relates to a method of partially plating a substrate for electronic devices, and is particularly suited to a method of partially plating selected portions, selectively, on a substrate for electronic devices on which semiconductor products are to be mounted.

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Background Art

In order to protect metallic portions of a substrate for electronic devices and easily bond the substrate to other electronic devices, selected portions of the metallic portions have heretofore been partially plated. There are various types of plating methods, and typical plating methods are wet electroplating and electroless plating.

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Wet electroplating is conducted by covering or masking portions other than selected portions in advance, and partially plating the selected portions. Wet electroplating, therefore, has the following problems: application to fine portions on a substrate for electronic devices on which semiconductor products are to be mounted is not suitable; and control of the plating amount is difficult.

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Moreover, wet plating has another problem in that plating cannot be performed unless the article to be plated is made electrically conductive. Furthermore, since wet electroplating uses large amounts of solutions such as a plating solution and a cleaning solution, it requires a large scale treating facility, which tends to cause an environmental problem.

On the other hand, since the electroless plating is

conducted with chemicals such as an acid or an alkali without utilizing electrolytic reactions, there arises the problem that the metals which can be used for plating are restricted.

5 Furthermore, in order to plate selected portions alone, the selected portions must be subjected to surface treatment; therefore, electroless plating has the problem that it requires many elaborate procedures. Still
10 furthermore, electroless plating has disadvantages in that it is difficult to form a thick plated layer and that the plating amount varies.

Disclosure of Invention

15 In view of the problems as mentioned above, the object of the present invention is to provide free control of the plating amount while easily determining a selected portion to be plated.

20 A method of partially plating a substrate for electronic devices according to the present invention comprises arranging small balls at selected portions of a substrate for mounting semiconductor devices thereon, or a
25 substrate for mounting electronic devices thereon and including a lead frame, and adhering or bonding the small balls thereto, and melting the small balls, thereby selectively plating the selected portions of the substrate
30 for electronic devices with a different metal.

35 Moreover, the method of partially plating a substrate for electronic devices according to the present invention is characterized by that the method comprises provisionally arranging and holding the small balls on an
40 arrangement base plate having through holes provided at positions corresponding to the portions to be plated of the substrate for electronic devices, transferring the arrangement base plate above the substrate for mounting
45 electronic devices, and adhering or bonding the small balls provisionally arranged at and held by the through holes to the portions to be plated, respectively.

Furthermore, in the provisionally arranging and holding procedure, excess small balls adhering to the arrangement base plate or the small balls which are provisionally held by the substrate are removed by
5 applying vibrations to the arrangement base plate, thereby provisionally arranging and holding the small balls.

Moreover, the vibrations are ultrasonic vibrations.

The present invention is further characterized in that the small balls are selected from solder, Sn alloy or
10 In alloy, and that the selected small balls are melted by reflowing to selectively plate the selected portions of the substrate for electronic devices with a different metal.

Moreover, the present invention is characterized in that the small balls are selected from Au, Ag, Pd, Pt, Ni
15 or Cr, and that the balls are melted by partial heating.

The present invention is further characterized in that the substrate for electronic devices is an insulating resin substrate or a polyimide tape, and that
20 the selected portions are wiring composed of copper.

Furthermore, the present invention is characterized in that the substrate for electronic devices is made of a ceramic material, and that the selected portions are wiring composed of copper.

25 Still furthermore, the present invention is characterized in that the substrate for electronic devices is a lead frame composed of copper or iron alloy, and that the leads of the lead frame are partially plated.

Since the present invention comprises the
30 technological means as mentioned above, metal balls provisionally arranged at selected portions of a substrate for electronic devices are melted, and as a result the metal balls are thermally diffused to produce firm adhesive force with the substrate metal. Since the metal
35 balls are bonded to the substrate metal by thermal diffusion, it is desirable that the metal balls be excellent in bonding caused by diffusion.

In addition, when a combination of the ball metal and the substrate metal shows a poor bonding force, or when the diffusion rate of the ball metal is too large, it is preferred to allow a metal different from the substrate metal and the ball metal to intervene between both metals.

Brief Description of Drawings

Fig. 1 shows a first embodiment of the present invention, and is a plan view of a glass-epoxy substrate which has leads of copper wiring formed thereon.

Figs. 2(a), 2(b) are views for illustrating the arrangement of small balls.

Fig. 3 shows a second embodiment of the present invention, and is a view illustrating a method of partially plating via holes of a TAB tape with solder.

Fig. 4 shows a third embodiment of the present invention, and is a view illustrating an example of a lead frame.

Best Mode for Carrying Out the Invention

One embodiment of the method of partially plating a substrate for electronic devices of the present invention will be explained below with reference to drawings.

Fig. 1 shows a first embodiment of the present invention, and is a view for illustrating partial plating of selected portions (ends) 3 of leads of copper wiring 2 on a glass-epoxy substrate 1.

The leads of copper wiring 2 in Fig. 1 have a wiring width of 50 μm . Balls 4 used for partially plating the selected portions 3 are solder balls, and have a diameter of 60 μm (eutectic solder).

When the method of partially plating the substrate for electronic devices in the present embodiment is carried out, firstly, the balls 4 are provisionally arranged at the ends 3 of the leads of copper wiring 2 on the glass-epoxy substrate 1.

Next, the balls 4 are reflowed at 290°C so that the

selected portions 3 of the leads of copper wiring 2 are plated with the balls 4 to achieve solder plating.

Next, a procedure of provisionally arranging the balls 4 at the ends 3 of the leads of copper wiring 2 will be explained with reference to Figs. 2(a), 2(b).

As shown in Figs. 2(a), 2(b), the balls 4 are arranged in the following manner. The back side of a 0.3 mm thick arrangement base plate 13 having holes 11, which have a diameter of 40 μ m, pierced through the plate at positions corresponding to the selected portions 3 of the leads of copper wiring 2 formed on the glass-epoxy substrate 1 is attracted by suction by applying a vacuum pressure (attracting mechanism not shown). The arrangement base plate 13 is brought close to a container 10 accommodating the balls 4 while the attracted state is being maintained.

The balls are attracted by suction and held at the respective holes 11. Excess balls adhere to portions other than the holes 11 of the arrangement base plate 13, or other excess balls adhere to the balls 4 attracted by suction to the holes 11 during attracting the balls by suction; therefore, the excess balls must be removed. In order to remove the excess balls, an arbitrary procedure such as a procedure in which vibrations are applied can be utilized. For example, the excess balls can be preferably removed by applying ultrasonic vibrations to the arrangement base plate 13 in the horizontal direction.

The selected portions 3 of the leads of copper wiring 2 and the holes 11 of the arrangement base plate 13 are subsequently relatively moved so that the holes 11 are located in correspondence with the selected portions 3, respectively, and the balls 4 are provisionally adhered to the selected portions 3 of the leads of copper wiring 2, respectively. The balls 4 are then melted by reflowing and are bonded to the selected portions 3 of the leads of copper wiring 2 as explained above.

Next, a second embodiment of the method of partially

plating a substrate for electronic devices of the present invention will be explained with reference to Fig. 3.

In the second embodiment, via holes 22 of a TAB tape 21 are plated with solder.

5 As shown in Fig. 3, small balls 24 are provisionally arranged on copper (Cu) wiring 23 exposed at a plurality of the via holes 22 formed at given positions of the TAB tape 21. In this case, the via holes 22 have a diameter of 100 μm , and the small balls 24 have a diameter of 60
10 μm . The number of the via holes 22 is, for example, about 300, and they are formed as one unit in a lattice-like form.

When a plurality of the small balls 24 are provisionally arranged as explained above, they are
15 subsequently reflowed, whereby the copper (Cu) wiring 23 exposed at the via holes 22 can be plated with solder easily and precisely.

Therefore, according to the method of partial plating in the present embodiment, wiring having a melting point
20 lower than that of the TAB tape 21 can be formed at the via holes 22. As a result, the copper (Cu) wiring 23 exposed in the via holes 22 of the TAB tape 21 and the electrodes of a semiconductor chip (not shown in the figure) can be bonded together at low temperature. It
25 becomes, therefore, possible to arrange electrodes in an area array-like form on an insulating tape.

Accordingly, the method of partially plating a substrate for electronic devices of the present embodiment is very favorable to the bonding of multi-pins. Moreover,
30 since the TAB tape 21 and the small balls 24 can be bonded together collectively using the arrangement base plate 13, the method can greatly improve the productivity of a large range of high density devices having a number of electrodes.

35 Next, a third embodiment of the present invention will be explained with reference to Fig. 4.

In the third embodiment, the method of partial

plating is applied to plating only the leads of a lead frame 31 with silver.

5 In the present embodiment, a silver ball (not shown in the figure) having a diameter of 150 μm is arranged at the end of each of the lead electrodes having a lead width of 150 μm , and provisionally adhered to the end. The silver ball is then spot-irradiated with a laser beam to be melted so that the end of the lead electrode is plated therewith.

10 Since partial plating is conducted as explained above in the method of partial plating in the present embodiments, selected portions of a substrate for electronic devices can be selectively plated with a different metal efficiently, and the plating amount can be controlled precisely.

15 That is, balls are arranged at selected portions of a substrate for electronic devices in the following manner. The back side of an arrangement base plate having holes formed at positions corresponding to the selected portions is attracted by suction by applying a vacuum pressure, whereby the balls are attracted by suction to and held by the holes, respectively. For example, about 300 balls can be arranged collectively.

20 Moreover, the plating amount of a selected portion can be controlled easily and precisely by adjusting the size of the ball. Furthermore, any metal can be used for plating so long as preparation of small balls of the metal is possible. The plating method also has an advantage of causing no environmental problem at the time of plating. 25 Still furthermore, the partial plating method of the present embodiments can be easily applied to plating two or more different layers in lamination.

Industrial Applicability

35 As explained above, small balls are provisionally arranged at portions to be plated, and melted so that the portions are plated with the metal in the present

invention. Accordingly, the present invention markedly improves the plating efficiency compared with conventional procedures where plating is conducted by depositing metal on an atomic or molecular scale.

5 Moreover, since the selectivity of portions to be plated is excellent, desired positions can be freely plated without conducting procedures such as masking portions not to be plated, and the plating operation can be greatly rationalized.

10 Moreover, the present invention has excellent advantages such as explained below. The plating amount can be easily and precisely controlled by adjusting the size of the balls. Furthermore, there is no fear of fouling the substrate for electronic devices and plating
15 can be conducted without environmental pollution because no plating solutions are used.

CLAIMS

1. A method of partially plating a substrate for electronic devices, comprising arranging small balls at selected portions of a substrate for mounting
5 semiconductor devices thereon, or a substrate for mounting electronic devices thereon and including a lead frame, and adhering or bonding the small balls thereto, and melting the small balls, thereby selectively plating the selected portions of the substrate for electronic devices with a
10 different metal.

2. The method of partially plating a substrate for electronic devices as claimed in claim 1, wherein the method comprises provisionally arranging and holding the small balls on an arrangement base plate having through
15 holes provided at positions corresponding to the portions to be plated of the substrate for electronic devices, transferring the arrangement base plate above the substrate for mounting electronic devices, and adhering or bonding the small balls provisionally arranged at and held
20 by the through holes to the portions to be plated, respectively.

3. The method of partially plating a substrate for electronic devices as claimed in claim 2, wherein, in the provisionally arranging and holding procedure, excess
25 small balls adhering to the arrangement base plate or the small balls which are provisionally held by the substrate are removed by applying vibrations to the arrangement base plate, thereby provisionally arranging and holding the small balls.

30 4. The method of partially plating a substrate for electronic devices as claimed in claim 3, wherein the vibrations are ultrasonic vibrations.

5. The method of partially plating a substrate for electronic devices as claimed in claim 1 or 2, wherein the
35 small balls are selected from solder, Sn alloy or In alloy and the selected small balls are melted by reflowing to selectively plate the selected portions of the substrate

for electronic devices with a different metal.

6. The method of partially plating a substrate for electronic devices as claimed in claim 1 or 2, wherein the small balls are selected from Au, Ag, Pd, Pt, Ni or Cr, and the balls are melted by partial heating.

7. The method of partially plating a substrate for electronic devices as claimed in claim 1 or 2, wherein the substrate for electronic devices is an insulating resin substrate or a polyimide tape, and the selected portions are wiring composed of copper.

8. The method of partially plating a substrate for electronic devices as claimed in claim 1 or 2, wherein the substrate for electronic devices is made of a ceramic material, and the selected portions are wiring composed of copper.

9. The method of partially plating a substrate for electronic devices as claimed in claim 1 or 2, wherein the substrate for electronic devices is a lead frame composed of copper or iron alloy, and the leads of the lead frame are partially plated.

ABSTRACT

The object of the present invention is to provide a free and precise control of the plating amount while easily determining a selected portion to be plated.

Small balls 24 are arranged at, and adhered or bonded to, via holes 22 of a TAB tape 21 and the small balls 24 are then melted so that a copper wiring 23 exposed at the via holes 22 of the TAB tape 21 can be selectively plated with a different metal to enable selected portions of a substrate for electronic devices to be partially plated easily and precisely.

Fig. 1

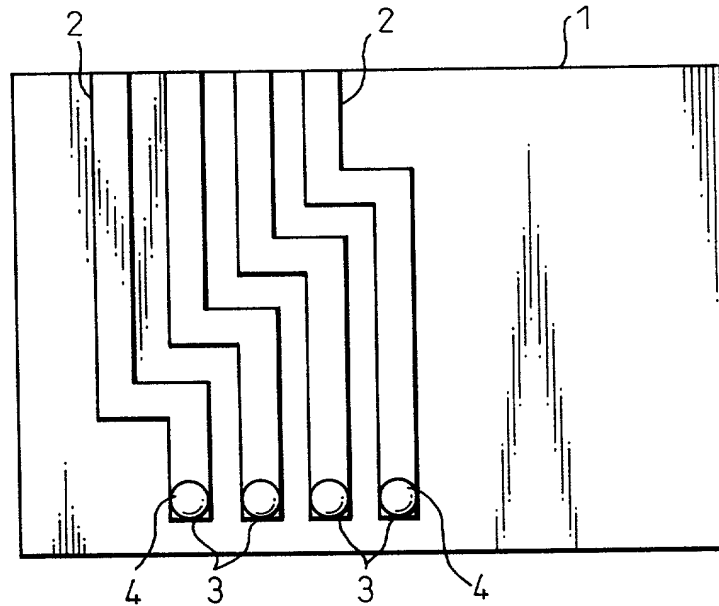


Fig. 2(a)

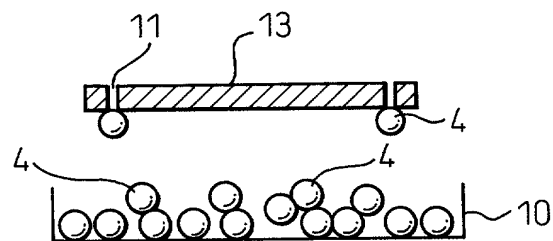


Fig. 2(b)

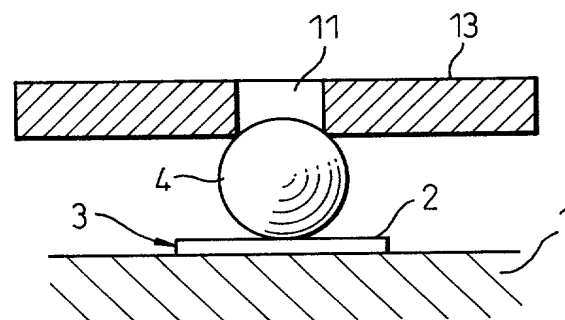


Fig. 3

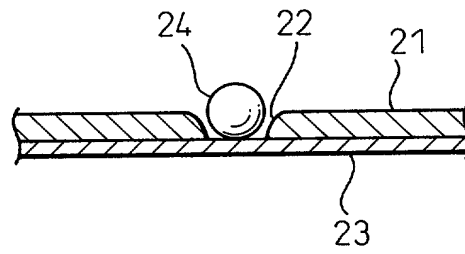
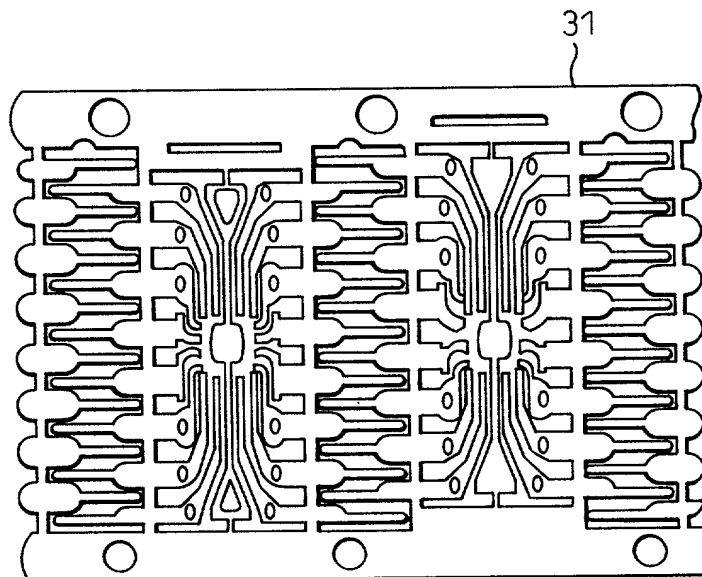


Fig. 4



Declaration and Power of Attorney For Patent Application

特許出願宣言書及び委任状

Japanese Language Declaration

日本語宣言書

下記の氏名の発明者として、私は以下の通り宣言します。

As a below named inventor, I hereby declare that:

私の住所、私書箱、国籍は下記の私の氏名の後に記載された通りです。

My residence, post office address and citizenship are as stated next to my name.

下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者であると（下記の名称が複数の場合）信じています。

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

METHOD OF PARTIALLY PLATING

SUBSTRATE FOR ELECTRONIC DEVICES

上記発明の明細書（下記の欄でx印がついていない場合は、本書に添付）は、

the specification of which is attached hereto unless the following box is checked:

☐ 月 日に提出され、米国出願番号または特許協定条約国際出願番号を _____ とし、
（該当する場合） _____ に訂正されました。

☒ was filed on August 27, 1997
as United States Application Number or
PCT International Application Number
PCT/JP97/02988 and was amended on
_____ (if applicable).

私は、特許請求範囲を含む上記訂正後の明細書を検討し、内容を理解していることをここに表明します。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

私は、運邦規則法典第37編第1条56項に定義されるとおり、特許資格の有無について重要な情報を開示する義務があることを認めます。

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

Japanese Language Declaration
(日本語宣言書)

私は、米国法典第35編119条(a)-(d)項又は365条(b)項に基づき下記の、米国以外の国の少なくとも一カ国を指定している特許協力条約365(a)項に基づく国際出願、又は外国での特許出願もしくは発明者証の出願についての外国優先権をここに主張するとともに、優先権を主張している、本出願の前に出願された特許または発明者証の外国出願を以下に、枠内をマークすることで、示しています。

Prior Foreign Application(s)

外国での先行出願 8-244268(Pat. Appln.)	Japan
(Number) (番号)	(Country) (国名)
(Number) (番号)	(Country) (国名)

I hereby claim foreign priority under Title 35, United States Code, Section 119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Priority Not Claimed

優先権主張なし

August 27, 1996
(Day/Month/Year Filed) (出願年月日)
(Day/Month/Year Filed) (出願年月日)

☐

☐

私は、第35編米国法典119条(e)項に基づいて下記の米国特許出願規定に記載された権利をここに主張いたします。

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below.

(Application No.) (出願番号)	(Filing Date) (出願日)
-----------------------------	------------------------

(Application No.) (出願番号)	(Filing Date) (出願日)
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私は、下記の米国法典第35編120条に基づいて下記の特許出願に記載された権利、又は米国を指定している特許協力条約365条(c)に基づき権利をここに主張します。また、本出願の各請求範囲の内容が米国法典第35編112条第1項又は特許協力条約で規定された方法で先行する米国特許出願に開示されていない限り、その先行米国出願書提出日以降で本出願書の日本国内または特許協力条約国際提出日までの期間中に入手された、運邦規則法典第37編1条56項で定義された特許資格の有無に関する重要な情報について開示義務があることを認識しています。

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s), or 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of application.

(Application No.) (出願番号)	(Filing Date) (出願日)
-----------------------------	------------------------

(Status: Patented, Pending, Abandoned) (現況: 特許許可済、係属中、放棄済)

(Application No.) (出願番号)	(Filing Date) (出願日)
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(Status: Patented, Pending, Abandoned) (現況: 特許許可済、係属中、放棄済)

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

委任状: 私は下記の発明者として、本出願に関する一切の手續きを特許商標局に対して遂行する弁護士または代理人として、下記の者を指名いたします。(弁護士、または代理人の氏名及び登録番号を明記のこと)

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith (list name and registration number)

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